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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,139	07/09/2003	Jung-Chien Chang	MR929-893	8097

4586 7590 04/18/2006

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EXAMINER	
LIN, JAMES	

ART UNIT	PAPER NUMBER
1762	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,139	CHANG, JUNG-CHIEN	
	Examiner	Art Unit	
	Jimmy Lin	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☒ Claim(s) 3 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claim 3 is objected to because of the following informalities: Claim 3 states "the first circuit layer is formed on the substrate in flat". This statement sounds awkward. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 4, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891), with teachings from Saijo et al. (US 6,579,565).

4. Regarding claim 1, Ito et al. discloses a method of manufacturing an integrated circuit package in Figures 6A to 7F. Copper leads 17 and insulating polyimide film 21 are deposited onto a substrate 11, as shown in Fig. 7E. The substrate is then removed by selective etching (column 5, lines 63 – 64) and a semiconductor chip (i.e. electronic

component) is attached to the integrated circuit package (column 6, lines 29 – 32). A resin 36 seals (i.e., encapsulates) the semiconductor (column 6, line 46). Ito et al. only discloses a single layer integrated circuit and does not teach depositing a resin-copper coating on the first circuit layer, forming a second circuit layer on the resin-copper coating, and electrically connecting the first and second circuit layers. However, Saijo et al. teaches that highly integrated assembly boards have been required to meet the demands of higher integration, more pins and less weight of semiconductor devices and that the demands are accomplished by developing multilayer circuit boards, thus improving the circuit integration (column 1, lines 20 – 25). One skilled in the art would have modified the integrated circuit in Ito et al. to form multilayers, thus forming an integrated circuit with higher integration. Neither Ito et al. nor Saijo et al. teaches the method of depositing a resin-copper coating on the first circuit layer, forming a second circuit layer on the resin-copper coating, and electrically connecting the first and second circuit layers.

Kurita et al. discloses a multilayer board with alternating resin layers and conductive layers (column 1, lines 65 – 67). Each resin layer may consist of a polyimide film (column 2, lines 3 – 4). Fig. 1 shows a plurality of polyimide films 11 – 16 and copper films 21 – 26. Each conductive layer is patterned in a predetermined configuration (column 5, lines 47 – 50). The conductive layers meet the limitations of a circuit layer since the conductive layers are deposited in a pattern and are electrically conductive. The polyimide film 11 is the substrate. A copper layer 21 (i.e., a first circuit layer) is deposited onto the substrate. Then a resin-copper layer is formed, wherein the

resin-copper layer is made up of a polyimide layer 12, a copper layer 22, and another polyimide layer 13. Another copper layer 23 (i.e., a second circuit layer) is deposited onto the resin-copper layer. Holes are formed in the resin layers and between the conductive layers and filled with electrically conductive material by plating or other means to electrically connect the various layers (column 5, lines 43 – 51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to manufacture an integrated circuit package with multiple layers. One would have been motivated to do so in order to form an interposer or motherboard that is capable of connecting to high-density packaging of terminals on semiconductors (column 1, lines 10 – 12).

Ito et al. also does not teach attaching electronic components to the topmost circuit layer. In Kurita et al., additional layers are further deposited onto the multilayer board, with a copper layer 26 being the topmost conductive layer (i.e., topmost circuit layer). Fig. 2b shows a semiconductor element 110 (i.e., an electronic component) connected to the multilayer board 1 at the topmost copper layer 26, as well as a motherboard 42 (i.e., an electronic component) connecting to the bottom of the multilayer board (column 5 line 64 – column 6 line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to connect an electronic component to the topmost circuit layer. One would have been motivated to do so in order to use the multilayer board as an interposer between two electronic components.

5. Regarding claim 3, Ito et al. describes the substrate as a laminated plate (column 4, lines 41 – 42). A plate can be defined as a smooth, flat, relatively thin body of uniform thickness. Thus, the limitation of a flat substrate is met.

6. Regarding claim 4, Kurita et al. discloses that holes are formed in the resin layers and between the conductive layers and filled with electrically conductive material by plating or other means to electrically connect the various layers (column 5, lines 43 – 51).

7. Regarding claim 17, Kurita et al. discloses a multilayered board with copper layer 23 being the second circuit layer. Fig. 1 further shows a resin-copper layer comprising of polyimide layers 14 – 16 and copper layers 24 - 25. Another copper layer 26 (i.e., a third circuit layer) is deposited onto the resin-copper layer. Holes are formed in the resin layers and between the conductive layers and filled with electrically conductive material by plating or other means to electrically connect the various layers (column 5, lines 43 – 51). Fig. 2b shows a semiconductor element 110 (i.e., an electronic component) connected to the multilayer board 1 at the topmost copper layer 26, as well as a motherboard 42 (i.e., an electronic component) connecting to the bottom of the multilayer board 1 (column 5 line 64 – column 6 line 5).

8. Claims 9, 11, and 12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891) and Saijo et al. (US 6,579,565) as applied to claims 1, 3, and 4 above, and further in view Farnworth (US 6,365,501). Ito et al. in view of Kurita et al. and Saijo et al. teach a method of preparing a multilayer board as discussed above, but do not teach connecting electronic

components to the second circuit layer by soldering tin balls. Ito et al. teaches in Fig. 1 that an integrated circuit package is formed such that the solder balls formed on the surface of the multilayer circuit board is connected to a circuit board (i.e., electronic component) in column 1, lines 39 – 4. Fig 7E shows projecting electrodes 23 formed of solder balls (column 5, lines 39 – 44). Solder balls are attached to the first conductive layer 17, which is the topmost conductive layer. The teaching of using solder balls in Ito et al. can be applied to the topmost circuit layer on the multilayer board in Kurita et al. Farnworth teaches that solder balls are generally formed of lead and tin and are used to join a chip to a carrier such as printed wiring board (column 3, lines 5 – 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply tin solder balls to the topmost circuit layer on a multilayer board. One would be motivated to do so in order to connect the multilayer board to a printed wiring board.

9. Claims 2 and 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891) and Saijo et al. (US 6,579,565) as applied to claims 1, 3, and 4 above, and further in view of Ikegami et al. (US 2003/0160339).

10. Regarding claim 2, Ito et al. in view of Kurita et al. and Saijo et al. fail to teach a substrate with dimples, whereby the first circuit layer at the dimples become protrusions after the substrate is removed. Ikegami et al. discloses a method of preparing an electronic component, wherein the substrate 15 has a plurality of fine holes in Fig. 4 (paragraph 33, lines 5 – 8) and electrically conductive protrusions are formed on portions of the conductive film (paragraph 13, lines 3 – 7). By definition, a hole can be

an indentation or depression. A dimple is also defined as a slight indentation or depression in a surface. The conductive protrusions then function as spacers in surface-mounting on an external printed wiring substrate through electrically conductive adhesive (paragraph 39, lines 4 – 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a substrate with dimples whereby the first circuit layer at the dimples become protrusions. One would be motivated to do so in order to provide spacers in the application of surface-mounting on a printed wiring substrate.

11. Regarding claims 5 – 8, Ito et al. in view of Kurita et al. and Saijo et al. do not teach the connecting of electronic components to the second circuit layer by bonding metal wires. However, Ikegami et al. discloses that electrode pads on a semiconductor chip are electrically connected to conductive films by bonding wires (paragraph 31, lines 17 – 20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to connect an electronic component to a circuit layer by bonding metal wires. One would have been motivated to do so in order to electrically connect the two devices at their respective conductive layers.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891), Saijo et al. (US 6,579,565), and Ikegami et al. (US 2003/0160339) as applied to claims 1 and 2 above, and further in view of and Farnworth (US 6,365,501). Ito et al. in view of Kurita et al., Saijo et al., and Ikegami et al. teach a method of preparing a multilayer board as discussed above, but do not teach connecting electronic components to the second circuit layer by soldering

tin balls. Ito et al. teaches in Fig. 1 that an integrated circuit package is formed such that the solder balls formed on the surface of the multilayer circuit board is connected to a circuit board (i.e., electronic component) (column 1, lines 39 – 4). Fig 7E shows projecting electrodes 23 formed of solder balls (column 5, lines 39 – 44). Solder balls are attached to the first conductive layer 17, which is the topmost conductive layer. The teaching of using solder balls in Ito et al. can be applied to the topmost circuit layer on the multilayer board in Kurita et al. Farnworth (US 6,365,501) teaches that solder balls are generally formed of lead and tin and used to join a chip to a carrier such as printed wiring board (column 3, lines 5 – 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply tin solder balls to the topmost circuit layer on a multilayer board. One would be motivated to do so in order to connect the multilayer board to a printed wiring board.

13. Claims 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891) and Saijo et al. (US 6,579,565), as applied to claims 1, 3, and 4 above, and further in view of Lin et al. (US 5,200,362) and Meyrat et al. (US 4,842, 536), with teachings from Carey et al. (US 5,672,260). Ito et al. in view of Kurita et al. and Saijo et al. do not teach applying isolating layers to the exposed first circuit layer. By definition, an isolating layer can be used to electrically insulate. Carey et al. teaches a method of depositing solder for direct chip attachment to a board or module (column 1, lines 30 – 36). In Fig. 3, a dielectric layer 30 is formed over a conductive layer 20, such that the dielectric layer is thick enough to contain the desired volume of solder material without

"mushrooming" over the surface of layer 30 (column 4 line 64 – column 5 line 3). Lin et al. discloses a method of fabricating a semiconductor device, wherein the substrate is removed and a protective coating 23 is applied to the exposed surface of the pattern of conductive traces 13 (column 3 line 66 – column 4 line 1). The protective coating can be an insulating film (column 3, lines 1 – 3). Openings 24 are formed through insulating film 23 to expose selected portions of the pattern of conductive traces (column 4, lines 3 – 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply an insulating film to the exposed first circuit layer. One would have been motivated to do so in order to provide an opening large enough to contain the solder without it "mushrooming" over the circuit layer.

Ito et al. in view of Kurita et al., Saijo et al., Carey et al., and Lin et al. do not teach applying tin-paste layers to the first circuit layer between adjacent isolating layers. However, Meyrat et al. discloses that a tin paste soldering material can be arranged on a circuit board where soldering is required and surface mounted devices are then connected with the tin paste (column 1, lines 12 – 29). Printed circuits manufactured in this way can accommodate more components per unit surface area (column 1, lines 30 – 33). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply tin paste to the selected portions of the exposed pattern of conductive traces in Lin et al. One would have been motivated to do so with the expectation of connecting the conductive traces to surface mounted devices in a space efficient manner.

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891), Saijo et al. (US 6,579,565), and Ikegami et al. (US 2003/0160339) as applied to claims 1 and 2 above, and further in view of Lin et al. (US 5,200,362) and Meyrat et al. (US 4,842, 536), with teachings from Carey et al. (US 5,672,260). Ito et al. in view of Kurita et al., Saijo et al., and Ikegami et al. do not teach applying isolating layers to the exposed first circuit layer. By definition, an isolating layer can be used to electrically insulate. Carey et al. teaches a method of depositing solder for direct chip attachment to a board or module (column 1, lines 30 – 36). In Fig. 3, a dielectric layer 30 is formed over a conductive layer 20, such that the dielectric layer is thick enough to contain the desired volume of solder material without "mushrooming" over the surface of layer 30 (column 4 line 64 – column 5 line 3). Lin et al. discloses a method of fabricating a semiconductor device, wherein the substrate is removed and a protective coating 23 is applied to the exposed surface of the pattern of conductive traces 13 (column 3 line 66 – column 4 line 1). The protective coating can be an insulating film (column 3, lines 1 – 3). Openings 24 are formed through insulating film 23 to expose selected portions of the pattern of conductive traces (column 4, lines 3 – 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply an insulating film to the exposed first circuit layer. One would have been motivated to do so in order to provide an opening large enough to contain the solder without it "mushrooming" over the circuit layer.

15. Ito et al. in view of Kurita et al., Saijo et al., Ikegami et al., Carey et al., and Lin et al. do not teach applying tin-paste layers to the first circuit layer between adjacent

isolating layers. However, Meyrat et al. discloses that a tin paste soldering material can be arranged on a circuit board where soldering is required and surface mounted devices are then connected with the tin paste (column 1, lines 12 – 29). Printed circuits manufactured in this way can accommodate more components per unit surface area (column 1, lines 30 – 33). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply tin paste to the selected portions of the exposed pattern of conductive traces in Lin et al. One would have been motivated to do so with the expectation of connecting the conductive traces to surface mounted devices in a space efficient manner.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Lin whose telephone number is 571-272-8902. The examiner can normally be reached on Monday thru Thursday 8 - 5:30 and Friday 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TIMOTHY MEEKS
SUPERVISORY PATENT EXAMINER